Sheet [3]: Internal Memory

[1] What are the different categories of computer memories? Briefly describe each category and list some examples.

[2] Briefly describe the different characteristics of computer memories.

[3] What are the differences among sequential access, direct access, and random access?

[4] What is the general relationship among access time, cost, and capacity of computer memories?

[5] What are the different types of semiconductor memories?

[6] What are the differences between RAM and ROM?

[7] What is the difference between DRAM and SRAM?

[8] Briefly describe the static RAM cell and the static ROM cell. Illustrate both the read and write operation.

[9] Briefly describe the ROM cell and illustrate both the read and write operation.

[10] What are the different types of ROM? Write a short description for each ROM type.

[11] What are the difference among EPROM, EEPROM, and flash memory?

[12] Answer the following:

a- How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?

b- How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?

c- How many lines must be decoded for chip select? Specify me size of the decoders.

[13] A computer uses RAM chips of 1024 x 1 capacity.

a- How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes?

b- How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus.

[14] A ROM chip of 1024 x 8 bits has four select inputs and operates from a 5-volt power supply. How many pins are needed for the IC package? Draw a block diagram and label all input and output terminals in the ROM.

[15] Extend the memory system of Fig.?? to 4096 bytes of RAM and 4096 bytes of ROM. List the memory-address map and indicate what size decoders are needed.

[16] A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.

a- How many RAM and ROM chips are needed?

b- Draw a memory-address map for the system.

c- Give the address range in hexadecimal for RAM, ROM, and interface.

[17] An 8-bit computer has a 16-bit address bus. The first 15 lines of the address are used to select a bank of 32K bytes of memory. The high-order bit of the address is used to select a register which receives the contents of the data bus. Explain how this configuration can be used to extend the memory capacity of the system to eight banks of 32K bytes each, for a total of 256K bytes of memory.

[18] A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K x 32.

a- Formulate all pertinent information required to construct the cache memory.

b- What is the size of the cache memory?

[19] The access time of a cache memory is 100 ns and that of main memory 1000 ns. It is estimated that 80 percent of the memory requests are for read and the remaining 20 percent for write. The hit ratio for read accesses only is 0.9. A write-through procedure is used.

a- What is the average access time of the system considering only memory read cycles?

b- What is the average access time of the system for both read and write requests?

c- What is the hit ratio taking into consideration the write cycles?

[20] A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.

a- How many bits are there in the tag, index, block, and word fields of the address format?

b- How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.

c- How many blocks can the cache accommodate?

[21] Suppose an 8-bit data word stored in memory is 11000010. Using the Hamming algorithm, determine what check bits would be stored in memory with the data word. Show how you got your answer.

[22] How many check bits are needed if the Hamming error correction code is used to detect single bit errors in a 1024-bit data word?

[23] A receiver receives the code 10010100101. When it using the Hamming encoding algorithm, has there been an error. If the error is occurred, which bit is in error?

« With my best wishes »

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